Notice of Allowability	Application No.	Applicant(s)	
	10/821,862	CHEN ET AL.	
	Examiner	Art Unit	
	Mujtaba K. Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *12/16/2005*.

2. ☒ The allowed claim(s) is/are *1-7*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

1/31/06

REASONS FOR ALLOWANCE

Claims 1-7 are allowed. The following is an Examiner's statement of reasons for allowance:

Independent claim 1 of the present application teaches a pre-stored digital word generator for producing multiple digital words, wherein the pre-stored digital word generator is applied to trigger a signal generating circuits of a plurality of test channels of a chip tester, the pre-stored digital word generator comprising: an edge memory used to store a primary preset information; an edge address counter electrically connected with the edge memory and used to point to an address of the edge memory; a reloadable down counter electrically connected with the edge memory for accessing the primary preset information of the address that is pointed by the edge address counter, wherein the reloadable down counter counts according to the primary preset information; and a plurality of word generating circuits electrically connected with the edge memory and the reloadable down counter, further comprising a rise register used to store a first register data of the secondary preset information; a fall register used to store a second register data of the secondary present information; a rising comparator used to compare the mark tag data of the primary preset information, which is pointed by the edge address counter, with the first register data to form a rising comparison result; a falling comparator used to compare the mark tag data of the primary preset information, which is pointed by the edge address counter, with the second register data to form a falling comparison result; and a latch component used to produce the trigger signals according to the rising comparison result and the falling comparison result; wherein the word generating circuits having a secondary present information, wherein the word generating circuits compares the primary and secondary preset information and then produce digital words for triggering the signal generating circuits according to the comparison result; and

every time when the reloadable down counter finishes its counting, the reloadable down counter triggers the edge address counter to make the edge address counter point to a next address of the edge memory and trigger the word generating circuits to make the word generating circuits output the digital words. The foregoing limitations are not found in the prior arts of record. The prior art of record, namely Parker, teaches test connectors that connect a circuit tester to an electronic device to be tested. The test vector matrix is divided into segments, each segment including one or more columns of the matrix. The unique vector segments within each matrix segment are stored in RAMs, one RAM for each test connector. A driver/comparator applies an electrical signal to some of the test connectors in response to a signal received from its associated RAM and receives an electrical signal on other of the test connectors and compares it to a signal received from the RAM. There is an independent sequencer for each matrix segment, each sequencer addressing the RAMs for that segment. A clock initiates and clocks the sequencers in synchrony to produce the test on the test connectors from the unique test vector segments stored in the RAMs. In particular, Parker teaches Figure 2 a circuit with a plurality of sequencers 61, such as 61A, 61B, etc., with each sequencer including a sequencer storage unit, such as 62A, a sequence directory unit, such as 66A, and a sequence controller, such as 70A. Each sequencer, such as 61A, is independent of the other sequencers 61 except for the common clock 76. Each sequencer, such as 61A, and its associated vector storage units, such as 56A and 56B, store an independently compressed segment of the complete test. When all the sequencers 61 are initiated and clocked in synchrony by clock 76 so that they run coincidently, the complete test is generated. None of the prior arts of record teach or fairly suggest all the limitations in the independent claim 1 of the present application. In particular, the limitations of "...a plurality of

word generating circuits electrically connected with the edge memory and the reloadable down counter, further comprising a rise register used to store a first register data of the secondary preset information; a fall register used to store a second register data of the secondary present information; a rising comparator used to compare the mark tag data of the primary preset information, which is pointed by the edge address counter, with the first register data to form a rising comparison result; a falling comparator used to compare the mark tag data of the primary preset information, which is pointed by the edge address counter, with the second register data to form a falling comparison result; and a latch component used to produce the trigger signals according to the rising comparison result and the falling comparison result; wherein the word generating circuits having a secondary present information, wherein the word generating circuits compares the primary and secondary preset information and then produce digital words for triggering the signal generating circuits according to the comparison result; and every time when the reloadable down counter finishes its counting, the reloadable down counter triggers the edge address counter to make the edge address counter point to a next address of the edge memory and trigger the word generating circuits to make the word generating circuits output the digital words." are not taught nor fairly suggested in the prior arts of record.

Independent claim 3 includes similar limitations of independent claim 1 and therefore is allowed for similar reasons.

Dependent claims 2 and 4-7 depend from independent claim 1 and inherently include limitations therein and therefore are allowed as well.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 571-272-3817. The examiner may normally be reached Mon – Thur 6:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 571-272-3819.

Mujtaba Chaudry
Art Unit 2133
January 31, 2006

ALBERT DECADY
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